IN THE UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company, Plaintiff, v. PANASONIC HOLDINGS CORP. et al., Defendants, ZT GROUP INT'L, INC., Defendant, ADVANTECH CO., LTD. Defendant, MICRO-STAR INTERNATIONAL CO., LTD. et al., Defendants, CISCO SYSTEMS, INC. Defendant.	**JURY TRIAL DEMANDED** **Civil Action No. 6:23-cv-00880-ADA** **Civil Action No. 6:23-cv-00881-ADA** **Civil Action No. 6:23-cv-00882-ADA** **Civil Action No. 6:23-cv-00883-ADA** **Civil Action No. 6:23-cv-00884-ADA**

DEFENDANTS' COORDINATED REPLY CLAIM CONSTRUCTION BRIEF

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74	Universal Serial Bus Specification, Revision 2.0, April 27, 2000

I. INTRODUCTION

For the reasons set forth in their Opening Brief and for the additional reasons discussed herein, Defendants respectfully submit that their proposed constructions should be adopted for all disputed claim terms.[1]

II. ACQIS IS PRECLUDED FROM RE-LITIGATING THE *EMC* CONSTRUCTIONS

ACQIS should be precluded from re-litigating the EMC constructions for the reasons set forth in Defendants' Opening Brief. ACQIS has not pointed to anything in its responsive brief that should alter that result.

III. DISPUTED CLAIM TERMS

A. "low voltage differential signal (LVDS) [channel]" / "LVDS [channel]"

'436 Patent (cls. 13, 14); '977 Patent (cls. 1, 6, 7, 11); '359 Patent (cls. 6, 7, 19); '797 Patent (cls. 36, 38); '768 Patent (cls. 1–7, 9, 10, 13-16, 33-35, 39, 40); '769 Patent (cl. 19); '750 Patent (cls. 1, 2, 4–7, 10, 11, 21, 24–27, 29, 31, 35, 37, 38, 44–48); '654 Patent (cls. 20, 21, 23, 24); '739 Patent (cls. 18, 20, 21, 26, 33, 36); '140 Patent (cls. 14, 17, 30, 31, 35); '947 Patent (cls. 14, 19, 29, 35, 48, 54).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"[a channel for carrying] a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3"	Plain and ordinary meaning.

ACQIS points to various examples of allegedly *generic* LVDS technologies that do not adhere to the ANSI or IEEE standards. However, none of these examples support ACQIS' position. For example, ACQIS points to a technology called "HyperTransport" which purported to use a type of low voltage differential signaling, but "not the conventional IEEE LVDS standard." Resp. Br., 12; *see also* Ex. 60 at 11. It should first be noted that the same white paper describes HyperTransport as an "enhanced LVDS technique developed to evolve with the performance of

[1] The identical reply brief is being filed in each of the cases in the above caption.

future process technologies" (Ex. 60 at 11), and so it is not surprising that it would include additional features, beyond the basic requirements of the standards. But more to the point, the white paper confirms that *conventional* LVDS was defined by the standards. *See id.* (referring to "the conventional IEEE LVDS standard"). Additional features might be added, but the standards represent the baseline. The fact that the patents purport to use the term LVDS "to generically refer to low voltage differential signals" as opposed to "any particular type of LVDS technology" is wholly consistent with this understanding.

Similarly, ACQIS relies on the VESA Plug-and-Display (PD) standard and its discussion of Transition Minimized Differential Signaling (TMDS). According to ACQIS and its expert, the TMDS technology was "not tethered to any specific LVDS standard." Resp. Br., 12. However, when describing the characteristics of the TMDS interface, the VESA standard does not actually use the proper term "LVDS." Rather, it uses the more generic term "low-swing differential voltage," as reproduced below:

> The TMDS interface takes parallel data from the host graphics controller and transmits it serially at high speed to the receiver.
>
> The characteristics of this interface are:
>
> - Uses 3 differential data pairs with timing and control data embedded in data transmission.
> - Uses transition controlled binary DC balanced coding for reliable, low-power, and high-speed data transmission.
> - Uses low-swing differential voltage.

Ex. 57 at 31.

The materials cited by ACQIS confirm that i) *conventional* LVDS was understood in reference to established standards (*e.g.* ANSI and IEEE); and ii) persons skilled in the art used different, more generic verbiage when describing interfaces that did not adhere to those standards.

Accordingly, the LVDS terms should be construed with reference to the ANSI and IEEE standards, as they would have been understood by a POSITA.

B. "Peripheral Component Interconnect (PCI) [/PCI] bus transaction"

'436 Patent (cls. 13-14); '797 Patent (cls. 36, 38); '768 Patent (cls. 1-7, 9-10, 13-16, 33, 35, 39); '750 Patent (cls. 1-2, 5-6, 10-11, 21, 25-27, 29, 31, 35, 38, 44-47); '654 Patent (cls. 21, 24); '977 Patent (cl. 1); '359 Patent (cl. 7); '140 Patent (cl. 30); '947 Patent (cls. 19, 29, 35, 48, 54).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"a transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"

ACQIS is wrong in claiming that "*EMC* addressed different issues of claim scope than the claims presented here." Resp. Br., 5. The *EMC* court explicitly construed "Peripheral Component Interconnect (PCI) [/PCI] bus transaction" as its own claim term before construing the "different phrases … which use the term 'PCI bus transaction.'" *ACQIS, LLC v. EMC Corp.*, 2017 WL 6211051, at *5, 8 (D. Mass. Dec. 8, 2017) ("*EMC* Markman Order"). Thus, at a minimum, the issues concerning the "PCI bus transaction" term itself are the same and issue preclusion applies.[2]

Turning to the actual *EMC* construction, it is clear that the district court and the Federal Circuit limited "PCI bus transaction" to a ***single*** category of transactions -- transactions "in accordance with the industry standard PCI Local Bus Specification." *ACQIS, LLC v. EMC Corp.,* 2022 WL 1562847, at *1 (Fed. Cir. 2022); Dkt. 53-44 at 17-18 ("specifically adopt[ing] the district court's constructions of the terms 'Peripheral Component Interconnect (PCI) bus transaction,' … and related terms" in the *EMC* Markman Order). ACQIS's proposed modification is inconsistent

[2] Defendants maintain their position that issue preclusion applies to the other PCI related terms as nothing in Plaintiff's Responsive Brief properly rebuts Defendants' arguments set out between pages 2 and 6 of their Opening Brief.

with the Federal Circuit's construction because it adds a second, *alternative*, category of transactions to that construction: a transaction [1] in accordance ***or [2] backwards compatible*** with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component. ACQIS does not dispute that "*or* backwards compatible" is written as an alternative to the "in accordance" portion in its construction. Instead of addressing the disjunctive nature of its proposal, ACQIS simply argues that "adding 'backwards compatibility" does not expand the claim scope" without addressing the "or" portion of the construction. Resp. Br., 16-17 (citing to *Sony*, Dkt. 69 at 3 (W.D. Tex. Sept. 6, 2023); Ex. 63, *ASUSTeK*, Dkt. 124 (Transcript of Sept. 1, 2022, Hearing) at 36:6-16 (W.D. Tex. Sept. 2, 2022)).

Because a "backwards compatible" transaction is an ***alternative*** to transactions "in accordance with" the PCI Specification, the addition of "or backwards compatible" to the Federal Circuit construction will encompass other transactions not in accordance with the PCI Specification. This completely contradicts the Federal Circuit's construction because a "backwards compatible" transaction would improperly expand the scope of "PCI bus transaction" beyond the limits set by the Federal Circuit, which this Court may not do. *See*, *e.g.*, *Eolas Techs., Inc. v. Adobe Sys., Inc.*, No. 09-CV-446, 2011 WL 11070303, at *2 (E.D. Tex. Sept. 23, 2011) (acknowledging Federal Circuit constructions as binding).

Moreover, if the Federal Circuit's construction of "in accordance with" already encompassed "backwards compatibility" transactions (as ACQIS suggests), there would be no need to amend the construction at all. Alternatively, ACQIS could have proposed a conjunctive construction, such as "***and*** backwards compatible" with, if it were really only seeking to clarify the meaning of the term. Likewise, if ACQIS alleges that "backwards compatible" means that it

"achieves backwards compatibility with PCI legacy devices," Resp. Br., 18-19, then it could have included such language in its construction. But ACQIS chose to do neither.

ACQIS's claim that "'backwards compatibility' is well-supported by the intrinsic record" (Resp. Br., 17-18) is a red herring as ACQIS confuses what (if any)[3] backwards compatibility is taught by the Asserted Patents. The language ACQIS cites simply confirms that any reverse compatibility contemplated by the Asserted Patents is allowing the transmission of existing PCI bus transactions (i.e., one's that meet the industry standard PCI Local Bus Specification) over a new ***wiring scheme*** (serial instead of parallel, using LVDS). ACQIS confuses that purported reverse compatibility (which conveys the industry standard PCI Local Bus Specification transaction over the new wiring scheme) with reverse compatibility of the PCI bus transaction itself. Reverse compatibility of the PCI bus transaction ***itself*** is not contemplated by the Asserted Patents as confirmed by the evidence cited by ACQIS and its expert that focuses on replacing parallel wiring for serial LVDS channels in an XPBus that interfaces two PCI or PCI-like buses. Resp. Br., 18.[4]

In other words, any reverse compatibility contemplated by the Asserted Patents would involve: starting with an industry standard PCI Local Bus Specification transaction, serializing that transaction, sending it down LVDS lines, and then reassembling the serialized information back into the industry standard PCI Local Bus Specification transaction. This means that there must be a transaction in accordance with the industry standard PCI Local Bus Specification ***before***

[3] ACQIS tacitly admits that "backwards compatible" does not appear in the Asserted Patents with its statement that "[r]egardless of whether the words 'backwards compatible' appear in the Asserted Patents, the ***concept*** of backwards compatibility certainly does." Resp. Br., 17-18 (emphasis added) (citing to the Sahan Declaration, which is not intrinsic evidence).

[4] ACQIS' arguments that previous courts have construed the claims as not requiring a PCI bus is misdirection. Resp. Br., 18. The claim term at issue relates to the transaction being conveyed by hardware, not the hardware itself.

the hardware of the purported invention can convey/communicate it over the LVDS lines. There is simply no disclosure or suggestion of using a transaction that is not in accordance with the industry standard PCI Local Bus Specification over the allegedly novel XPBus.

Finally, ACQIS is wrong in claiming that its "statements to the PTAB have no bearing on the inclusion of 'or backwards compatible' in the construction of 'PCI bus transaction.'" Resp. Br., 19. If ACQIS believed "backwards compatible" was within the scope of "PCI bus transaction," surely it would have argued as much in the IPRs. Regardless, ACQIS made repeated, unequivocal statements as to what it believed "PCI bus transaction" means and even agreed to Defendants' construction in prior litigation without any mention of "backwards compatible." *See* Def.s' Opening Br. at 15-17. Accordingly, ACQIS should be held to its prior statements, which is another reason why the Court should adopt Defendants' construction.

C. "convey [/conveying/conveys/communicating/communicate/transmitting] … a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]"

'436 Patent (cls. 13-14); '797 Patent (cls. 36, 38); '768 Patent (cls. 1-7, 9-10, 13-16, 33, 35, 39); '750 Patent (cls. 1-2, 5-6, 10-11, 21, 25-27, 29, 31, 35, 38, 44-47); '654 Patent (cls. 21, 24); '977 Patent (cl. 1); '359 Patent (cl. 7); '140 Patent (cl. 30); '947 Patent (cls. 19, 29, 35, 48, 54).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"communicating a PCI bus transaction, including all address, data, and control bits"	"conveying"/"conveys"/"communicating"/"communicate"/ "transmitting": plain and ordinary meaning. "conveying"/"conveys"/"communicating"/"communicate"/ "transmitting" specific bits (e.g., address bits, data bits, and/or byte enable information bit) of a "PCI bus transaction": The EMC construction for "communicating … PCI bus transaction" does not apply to these terms.

Defendants' construction for this term should be adopted for the reasons set forth in Defendants' Opening Brief. ACQIS has not pointed to anything in its responsive brief that should

alter that result. Therefore, Defendants respectfully request that Court adopt the Defendants' proposed construction for this term.

D. Claims reciting a [Peripheral Component Interconnect] PCI bus transaction, or an encoded [Peripheral Component Interconnect] PCI bus transaction, "in [a] serial form" or "serially encoded" or "in a serial bit stream"

'436 Patent (cl. 13); '797 Patent (cl. 36); '768 Patent (cls. 1, 3-4, 6-7, 10, 13, 15, 39); '750 Patent (cls. 1, 5, 10, 21, 25, 27, 29, 31, 35, 44, 46); '654 Patent (cls. 21, 24); '977 Patent (cl. 1); '359 Patent (cl. 7); '140 Patent (cl. 30); '947 Patent (cls. 19, 29, 35, 48, 54).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a PCI bus transaction that has been serialized from a parallel form"	"encoded", "serial[ly]": plain and ordinary meaning. The *EMC* construction of "[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms applies only to certain claims and terms, *i.e.,* "claims reciting an 'encoded' PCI bus transaction" and more specifically, terms that recite (1) "encoded," (2) "serial," and (3) "PCI bus transaction,"

Defendants' construction for this term should be adopted for the reasons set forth in Defendants' Opening Brief. ACQIS has not pointed to anything in its responsive brief that should alter that result. Therefore, Defendants respectfully request that Court adopt the Defendants' proposed construction for this term.

E. "of [a] Peripheral Component Interconnect (PCI) bus transaction [/of [a] PCI bus transaction]"

'436 Patent (cls. 13-14); '797 Patent (cls. 36, 38); '768 Patent (cls. 1-7, 9-10, 13-16, 33, 35, 39); '750 Patent (cls. 1-2, 5-6, 10-11, 21, 25-27, 29, 31, 35, 38, 44-47); '654 Patent (cls. 21, 24); '977 Patent (cl. 1); '359 Patent (cl. 7); '140 Patent (cl. 30); '947 Patent (cls. 19, 29, 35, 48, 54).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"of a": plain and ordinary meaning.

None of ACQIS's arguments against Defendants' proposed construction can overcome the overwhelming evidence that the specific bits must be from a PCI bus transaction in accordance with the PCI specification.

First, Defendants' proposed construction does not remove context or read out the recitation of specific bits of a PCI bus transaction. The recitation of specific bits always precedes the term under construction, so nothing is read out and no context is lost.

Specifically, the term being construed has two permutations: "of [a] Peripheral Component Interconnect (PCI) bus transaction" and "of [a] PCI bus transaction." The specific bits recited immediately before the term being construed have two formats: "***address and data [bits]***" and "***address bits, data bits, and byte enable information bits.***" Resp. Br., 28. Therefore, as an example, as properly construed according to the Defendants' construction, the first format would read in full: "address and data [bits] ***from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.***" The second format would read in full: "address bits, data bits, and byte enable information bits ***from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.***" The specific bits remain, and only those bits are required to be conveyed or transmitted as called for in the claims reciting conveyance/transmission of those specific bits. With Defendants' construction, it is only the specific bits (which originate from a PCI bus transaction) that are required to be conveyed/transmitted, which is literally what the claims recite. The fact that a PCI bus transaction exists (from which the specific bits originate) is unambiguously required by the claims (as further addressed below).

Notably, ACQIS does not propose a construction for the recited bits themselves other than plain meaning, tacitly admitting there is no need to construe the recited bits. More importantly, including the recited bits as part of the term being construed changes nothing because the recited bits always immediately proceed the term being construed (see first and second format examples above where the specific bits are paired with the Defendants' construction).

Second, ACQIS admits that for those claims that separately reference conveying/transmitting "the PCI bus transaction," in all instances, "the PCI bus transaction" refers to the limitation reciting specific bits of a PCI bus transaction. Resp. Br., 29. Defendants agree. There is no antecedent basis for "the PCI bus transaction" other than "of [a] Peripheral Component Interconnect (PCI) bus transaction" or "of [a] PCI bus transaction." But, ACQIS goes on to argue that if there is any limitation construed to require a complete PCI bus transaction, that is a separate limitation independent of the limitation reciting conveyance/transmission of specific bits "of a PCI bus transaction." *Id.* This argument contradicts ACQIS's admission and the plain wording of the claims.

Taking claims 36 and 38 of the '797 patent as an example, claim 36 recites:

> "configuring the interface controller to adapt to different numbers of differential signal line pairs for conveying encoded address and data bits ***of a Peripheral Component Interconnect (PCI) bus transaction*** in serial form."

Claim 38 depends upon claim 36, and recites:

> "configuring the interface controller to generate different data transfer frequencies ***to convey the PCI bus transaction*** through the LVDS channel based on different clock frequencies generated by the PLL clock circuitry."[5]

[5] There are over three dozen other dependent claims that similarly recite "to convey the PCI bus transaction" where the only antecedent basis is a parent claim reciting specific bits of a PCI bus transaction: '768 patent, claims 3, 6, 11, 12, 14, 17, 19-21, 23, 25, 28-29, 31-32, 35, 38; '750 patent, claims 2-3, 6, 11, 16-17, 19, 22-23, 26, 28, 30, 32-33, 37-38, 45, 47; '947 patent, claims 25, 41, 55, 59.

Claim 38 recites "to convey ***the PCI bus transaction***." Therefore, claim 38 requires a PCI bus transaction to exist, and to be conveyed. Yet, the only antecedent basis for "the PCI bus transaction" is in parent claim 36 where it recites "***of a Peripheral Component Interconnect (PCI) bus transaction.***" ACQIS admits that "the PCI bus transaction" of claim 38 refers to "encoded address and data bits ***of a Peripheral Component Interconnect (PCI) bus transaction***" in claim 36. Resp. Br., 28.

Further, the plain language of claim 36 requires the conveyed encoded address and data bits be "of" that PCI bus transaction. Therefore, claim 36 requires there to be a PCI bus transaction, and the encoded address and data bits be of (from) that transaction, even though conveyance of that PCI bus transaction is later claimed in claim 38. Otherwise, claim 38 has no antecedent basis and is rendered meaningless. Consequently, ACQIS is simply wrong to say claim 38 requires a PCI bus transaction, "the PCI bus transaction" of claim 38 is referring to "of a Peripheral Component Interconnect (PCI) bus transaction" in claim 36, but somehow claim 36 does not require a PCI bus transaction nor that the address and data bits originate from that PCI bus transaction.

Claim 1 of the '797 patent provides another compelling example, which states:

> "conveying encoded address and data bits ***of a Peripheral Component Interconnect (PCI) bus transaction*** in serial form over the serial channels ***to preserve the PCI bus transaction***;"[6]

Once again, it cannot be disputed that "the PCI bus transaction" refers to the limitation "of a Peripheral Component Interconnect (PCI) bus transaction." Yet, ACQIS wrongly maintains that the "conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus

[6] Other examples of this claim language include: '797 patent, claims 4, 7, 10, 14, 18, 21; '654 patent, claims 14, 17, 26, 29, 32, 35.

transaction" does not require a PCI bus transaction to exist, even though the claim expressly recites "to preserve the PCI bus transaction" and the only antecedent basis for "the PCI bus transaction" is "of a Peripheral Component Interconnect (PCI) bus transaction." ACQIS does not, nor can it, explain how a PCI bus transaction is preserved yet is not required to exist in the first place. The claims unambiguously require a PCI bus transaction, and that the address and data bits originate from it, otherwise "the PCI bus transaction" being preserved lacks all meaning. Tellingly, ACQIS cites to no support or embodiment in the Asserted Patents where the address and data bits being conveyed according to invention do not originate from a PCI bus transaction.

The Court should also reject ACQIS' arguments and construction, because adopting them would effectively invalidate scores of claims. The claims of the Asserted Patents recite "the PCI bus transaction" more than 60 times, and every time the sole antecedent basis is "of [a] Peripheral Component Interconnect (PCI) bus transaction" or "of [a] PCI bus transaction." If "of [a] Peripheral Component Interconnect (PCI) bus transaction" and "of [a] PCI bus transaction" do not provide antecedent basis for and thus require the existence of the subsequently recited "the PCI bus transaction" (and that the specific bits "of" that transaction originate from that transaction), then over 60 claims of the Asserted Patents are rendered invalid as indefinite for lacking antecedent basis.[7]

F. "console"

'768 Patent (cl. 34); '750 Patent (cls. 5, 10, 24, 35, 44, 48); '654 Patent (cls. 20, 23); '977 Patent (cl. 1); '359 Patent (cls. 6, 19); '739 Patent (cls. 18, 36); '140 Patent (cls. 14, 31).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a chassis that connects several components of a computer system"	"a chassis or enclosure, housing one or more coupling sites, that connects components of a computer system"

[7] In Footnote 9, ACQIS criticizes Defendants for pointing to claims that are not asserted. But there is no support for ACQIS's suggestion that the proper construction of claim terms can change depending on which claims are asserted.

Defendants' construction for this term should be adopted for the reasons set forth in Defendants' Opening Brief. ACQIS has not pointed to anything in its responsive brief that should alter that result. Therefore, Defendants respectfully request that Court adopt the Defendants' proposed construction for this term.

G. "USB" / "Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol data[/information]"

'768 Patent (cls. 34, 40); '750 Patent (cls. 4, 7, 24, 46, 48); '654 Patent (cls. 20, 23); '977 Patent (cls. 1, 11); '359 Patent (cls. 6, 19); '739 Patent (cls. 18, 20, 26, 33, 36); '947 Patent (cl. 14); '769 Patent (cl. 19).	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard"	Plain and ordinary meaning.

Contrary to ACQIS's position, Defendants are not asking the Court to depart from its prior constructions in the *Sony* and *ASUSTeK* cases. However, the Court should clarify that the references to USB in the claims *must* be limited to standards (or proposed standards) at the time of the invention, as it did in *Atlas Global Techs. LLC v. Zyxel Networks Corp.* No. 6-22-cv-355-ADA, 2023 U.S. Dist. LEXIS 81575, 2023 WL 3361214, at *18 (W.D. Tex. May 9, 2023) (limiting construction of "a mode that is high efficiency" to refer to standards or proposed standards "at the time of the invention.").

It is well-known that claims must be given their meaning "at the time of the invention," or, more simply put, a claim cannot have different meanings at different times. *See Phillips*, 415 F.3d at 1313; *PC Connector Sols. LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005). This Court has recognized that in the context of industry standards, claim terms that use standards-based language refer to standards "at the time of invention." *Atlas Global Techs.*, 2023 WL 3361214 at

*18 (citing *Uniloc USA, Inc. v. Apple, Inc.*, No. 19-cv-01692-EJD, 2021 U.S. Dist. LEXIS 25603, 2021 WL 432183, at *8-*9 (N.D. Cal. Jan. 15, 2021)).

The terms in the asserted patents that include "USB" should be clarified to explain that the plain and ordinary meaning limits USB to the standards and proposed standards that existed at the time of the invention (and as described in the specification): USB 2.0 and prior versions. *See, e.g.*, '768 patent at 12:16–17. As an example, ACQIS admits that the "claims reference aspects of USB generally, e.g. '[USB] protocol data.'" Resp. Br., 32. The only 'USB protocol data' that existed at the time of the invention is protocol data included in USB 2.0 and earlier. Def.s' Opening Br., 33-34.

The fact that the physical interface transmits the data in opposite directions does not change the fact that the protocol data *must* be in accordance with USB 2.0 and earlier revisions. *Id.* Even though, as ACQIS argues, the claims recite an LVDS channel, the only "USB *information*" the LVDS channel could be communicating is USB 2.0 or earlier information (including USB 2.0 and earlier "protocol data packets," USB 2.0 and earlier "protocol data," and USB 2.0 and earlier "protocol information") as would be understood at the time of the invention. *Id.* at 31. USB 3.0 and 4.0 did not exist at the time of the invention (and ACQIS does not argue that either protocol existed, because it cannot), so a POSITA would understand that the only USB information the claims refer to is information in accordance with USB 2.0 and earlier revisions. *See generally,* Resp. Br.

ACQIS cannot expand the plain meaning of the claim to encompass ***modern*** USB standards beyond the standards in existence at the time of the invention. ACQIS did not invent USB standards, much less USB standards beyond USB 2.0. Therefore, references to the USB standards in the claims cannot refer to USB data, information, and protocols that did not exist in USB 2.0

and earlier revisions. ACQIS, throughout its briefing, carefully points to external components that utilize USB protocols and information in different ways, but never states that it modifies the USB specifications or standards referred to in the claim language. *See* Resp. Br., 30-33. As recognized in *Uniloc*, USB 2.0 protocols, standards, and information could remain in later standards, but (1) ACQIS does not argue that this is the case here, and (2) that does not change the fact that references in the claims to USB necessarily must be construed in accordance with a POSITA's knowledge at the time of the inventions, which here, would be the USB 2.0 and earlier standards or proposed standards at the time of the invention. 2021 WL 432183, at *8-*9.

As was the case in *Atlas Global Techs.,* here, Defendants' construction *clarifies* that the scope of the USB claim terms is what existed "at the time of invention" (USB 2.0 and earlier revisions) and *does not* impermissibly narrow the scope of 'USB' terms. 2023 WL 3361214 at *18.

H. "coupling the integrated CPU and interface device to a peripheral device attached to the motherboard through the LVDS channel with the adapted number of differential signal line pairs"

'797 Patent (cl. 36)	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
Indefinite	Plain and ordinary meaning.

ACQIS improperly relies solely on *ipse dixit* from its expert to provide meaning to the term "adapted number of differential signal line pairs." ACQIS repeatedly cites to the ***sole instance*** of the terms "adapt" or "adapted" in claim 36 itself, and, finding no support for its interpretation in the specification, file history, or chain of priority of the '797 patent, ACQIS merely presents conclusory testimony from its expert Dr. Sarhan. *See* Ex. 71 ¶¶ 78, 80, 87, 88, 91, 100, 101; *Horizon Pharma, Inc. v. Dr. Reddy's Lab'ys Inc.*, 839 F. App'x 500, 505 (Fed. Cir. 2021) ("Here, Appellants' expert merely made conclusory statements about what a skilled artisan would understand about the meaning of the claim term 'target' and quoted text from the patent's

specification that did not support this conclusion."); *IQASR LLC v. Wendt Corp.*, 825 F. App'x 900, 907–08 (Fed. Cir. 2020) ("[A] claim term does not become reasonably certain simply because a skilled artisan, when pressed, managed to articulate a definition for it.").

Rather than attempting to identify antecedent basis, ACQIS concedes that none exists and argues that no antecedent basis is necessary. Resp. Br. at 33–34 ("[t]he rigorous and formulaic patent drafting conventions are not at issue here."). But in the face of missing antecedent basis, the law requires an inquiry into whether the specification "clarif[ies] the meaning" of the claim. *Bushnell Hawthorne, LLC v. Cisco Sys., Inc.*, 813 F. App'x 522, 526 (Fed. Cir. 2020) (finding that "[t]he specification does not clarify the meaning" after determining that "'said different IP Address' appears in the claim without antecedent basis" because "[t]he lack of antecedent basis signals a potential indefiniteness problem but does not end the inquiry."). Here, the specification provides no guidance regarding "***the adapted number*** of differential signal line pairs" claim language, and thus advocates for an indefiniteness finding. ACQIS tellingly makes exceptionally few cites to the specification of the '797 patent, even though "the specification is always highly relevant to the claim construction analysis…. [I]t is the single best guide to the meaning of a disputed term." *Cont'l Cirs. LLC v. Intel Corp.*, 915 F.3d 788, 796 (Fed. Cir. 2019) (internal quotation omitted).

Without any support in the intrinsic record, ACQIS and its expert attempt to navigate the indefiniteness issue by rewriting the claim to support their interpretation. ACQIS argues that "completing the coupling 'with the adapted number of differential signal line pairs' is plainly the next step after the initial configuration of the line pairs" (Resp. Br.at 34) impermissibly revising the claim to recite three steps instead of two.

First, ACQIS admits the prior "configuring" step does not require any "initial configuration" of a ***specific number of*** differential signal line pairs. Rather, as ACQIS's chart states, the claim only requires "configuring the ***interface controller to adapt*** to ***different numbers***"—plural—"of differential signal line pairs." In other words, the prior limitation requires configuring an interface controller to be capable of adapting to many different numbers of differential signal line pairs, not to a ***specific*** number of pairs. Resp. Br. at 35 ("the interface controller is designed so that it supports multiple LVDS channels and ***can*** then adapt to a specific number of LVDS channels.") (emphasis added).

ACQIS and its expert then rewrite the term at issue, injecting a step in which "a determination is made as to the specific number of LVDS channels to use" – but no such language appears in the claim. Resp. Brief at 35. ACQIS effectively reads the term in question as three separate steps: (1) connecting the integrated CPU and interface device to a peripheral device attached to the motherboard through ***a*** number of differential signal line pairs; and (2) the interface controller ***determining the*** number of LVDS pairs; and (3) ***adapting to the*** number of differential signal line pairs. But a plain reading of the claim language provides no support for this interpretation—there is no discussion of a separate determination step at all, and as discussed above, no claimed step of the interface controller adapting to ***any specific number*** of LVDS pairs.

Second, the specification also does not support ACQIS's interpretation. *See* Ex. 71 ¶ 75 referring to '797 patent 24:61-64, ¶ 81 referring to '797 patent 5:54–64 and 19:3–11. Rather, those passages merely state that "[t]he CPU bridge component … operates to couple the high speed CPU main bus 1764 to specialty buses ***of varying speeds and capability*** that connect to other computer components," which simply describes the connection between the CPU bus and interface controller, ***not*** the ability of the interface controller to "adapt to different numbers of differential

signal line pairs." Additionally, "varying speeds and capability" can be achieved in many other ways than increasing the number of differential signal line pairs, *e.g.*, with clock speed variation, encoding schemes, or variable packet sizes, none of which appear in claim 36. Furthermore, the exemplary CPU bridge which the immediately following passage of the specification refers to, the 82443LX PCI/AGP Controller from Intel ('797 patent 25:1–3), has no such adaptability with respect to its PCI connection. Ex. 73 at 9, 12 (a "32-bit PCI Bus Interface" that "supports only synchronous PCI coupling to the host bus frequency").

ACQIS manufactures support for its interpretation in the specification where none exists. It is undisputed that the specification does not describe the use of fewer than four differential signal line pairs when certain peripheral devices are connected. (Ex. 71 ¶ 87.) ACQIS's expert implausibly argues that this absence of detail is intentional, stating, "[i]nstead of giving an example with only one LVDS channel … the specification provides a more complex example with four LVDS channels for conveying data." *Id*. ¶ 85. In fact, this "more complex example" is the ***only*** example in the specification. There is simply no support in the specification for ACQIS's interpretation that the XPBus is configurable to use fewer than four LVDS channels. *See Horizon Pharma, Inc.*, 839 F. App'x at 505; *IQASR LLC*, 825 F. App'x at 907–08.

Finally, ACQIS's reliance on the intrinsic record, particularly as it relates to USB 2.0, is fatally misguided, because it is, at a physical level, directly at odds with the claim language of claim 36. USB 2.0 is fundamentally limited to a single pair of differential signal lines—it cannot "increase data throughput … by providing … multiple signal line pairs" as claim 36 recites—and relying upon it to give structure to the term "the adapted ***number of differential signal line pairs***" (*e.g.*, Resp. Br. at 36) is flatly illogical. *See* Ex. 74, USB 2.0 Revision at 86.

Thus, Defendants respectfully request that the Court find the disputed term "coupling the integrated CPU and interface device to a peripheral device attached to the motherboard through the LVDS channel with the adapted number of differential signal line pairs" to be indefinite.

I. "peripheral bridge"

'768 Patent (cls. 4, 10); '750 Patent (cl. 29); '654 Patent (cl. 23); '947 Patent (cl. 35)	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a component that interfaces with peripheral buses or peripheral devices"	Plain and ordinary meaning.

ACQIS does not explain why a construction it previously agreed to no longer "reflect[s] the plain … meaning" of this phrase or why it somehow has become "unnecessary." *See* Resp. Br., 37. While ACQIS argues that, in *Samsung*, it clarified that the peripheral bridge was a south bridge component, ACQIS did ***not*** find it necessary to add "south bridge" to the construction. Ex. 72 at 29. Moreover, ACQIS had no issue using the word "component" to construe "peripheral bridge" (*see id.*), although ACQIS now argues that "component" is a nonce word insufficient to convey the "function and relationship" of the term. *See* Resp. Br., 37–38.

Defendants' proposed construction specifies that "peripheral bridge" refers to a component *that interfaces* with peripheral buses or peripheral devices, plainly conveying the "function and relationship" that ACQIS claims is lacking. ACQIS also accuses Defendants of "add[ing] an unjustified limitation" to the term, *i.e.* interfacing *with peripheral buses or peripheral devices*. Resp. Br., 38. According to ACQIS, the claim language is not limited to interfacing with only these kinds of devices, but ACQIS does not explain or point to any examples of what else the term might include.

In its entirety, the construction is clear, supported by the intrinsic record, and will assist the jury in understanding ACQIS' claims. *See* Def.s' Opening Br. at 37–39. Therefore, the Court should adopt Defendants' proposed construction.

IV. CONCLUSION

Defendants respectfully request that the Court adopt their proposed claim constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on December 6, 2024, a copy of the foregoing document was served on the parties to this action by electronically filing true and correct copies with the Clerk of the Court using the CM/ECF system which will automatically send notification by e-mail of such filing to all counsel of record.

/s/ Matthew Blair
Matthew Blair